Code: 13A04301 **R13**

B.Tech II Year I Semester (R13) Supplementary Examinations November/December 2017

ELECTRONIC DEVICES & CIRCUITS

(Common to EEE, ECE & EIE)

Time: 3 hours Max. Marks: 70

PART – A

(Compulsory Question)

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1 Answer the following: (10 X 02 = 20 Marks)

(a) Define Mass action law.
(b) What is the need of filters in power supplies?
(c) State the differences between enhancement and depletion mode MOSFET.
(d) For a common emitter configuration if α is 0.975, then determine the value of β.
(e) Why thermal runaway occur in transistor?
(f) What is the need for biasing?
(g) State Miller's theorem.
(h) Draw the h parameter equivalent circuit of CE configuration.
(i) Mention the principle of operation of LED.
(j) Draw the symbol diagram and VI characteristics of Diac and Triac.

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT – I

2 For the P-type semiconductor silicon at 300 K if its conductivity is $1(\Omega\ cm)^{-1}$ given that mobility of holes in silicon is 500 cm^2/Vs. Find the concentration of electrons. Also determine the ratio of holes to the free electrons. It is given that the intrinsic concentration of silicon is 1.5×10^{10}.

OR

3 Discuss in detail about the working of bridge rectifier and derive all the parameters.

UNIT – II

4 Illustrate the working characteristics of CB configuration with neat circuit diagram.

OR

5 Draw and explain the construction and principle of operation of JFET and derive the relationship between pinch-off voltage and drain current.

UNIT – III

6 How to stabilize the Q-point using bias compensation techniques? Explain.

OR

7 State the reasons for biasing for zero current drift and derive the condition for zero drift. Also if the n-channel FET is biased at I_D = 0.8mA, calculate the value of $g_{m.}$ Given I_{DSS} = 1.65 mA , V_P = -2.0 V and g_{m0} = 1.60 mA/V.

UNIT – IV

8 A common collector circuit has the following components $R_1 = R_2 = 27\ k\Omega$, $R_E = 5.6\ k\Omega$, $R_L = 47\ k\Omega$, $R_S = 600\ \Omega$. The transistor parameters are $h_{ie} = 1\ k\Omega$, $h_{fe} = 85$ and $h_{oe} = 2\ \mu A/V$. Calculate A_i, R_i, A_v, R_0 using simplified hybrid model circuit.

OR

9 Draw the low frequency equivalent circuit of common source configuration of JFET with fixed bias and derive its performance parameters.

UNIT – V

10 Elaborate on the tunneling mechanism of Tunnel diode along with its VI characteristics.

OR

11 With the help of relevant schematic diagram, briefly describe the operational principle of UJT with its VI characteristics.

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