Code: 13A04504 **R13**

B.Tech III Year I Semester (R13) Supplementary Examinations November/December 2017

DIGITAL IC APPLICATIONS

(Electronics & Communication Engineering)

Time: 3 hours Max. Marks: 70

PART – A

(Compulsory Question)

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1 Answer the following: (10 X 02 = 20 Marks)

(a) What are the advantages and disadvantages of CMOS technology?
(b) List out the characteristics of ECL.
(c) What are the data types available in VHDL?
(d) What is binding?
(e) Write a VHDL program for 2×4 decoder.
(f) Write a VHDL program for 1×4 demultiplexer.
(g) What is structural style of modeling?
(h) Convert a D flip-flop into T flip-flop.
(i) Distinguish between SRAM and ROM.
(j) List out the applications of RAM.

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT – I

2 (a) With reference to the dynamic behavior of CMOS explain about speed and power dissipation of CMOS circuits.
(b) Design CMOS transistor circuit for 3-input AND gate. With the help of function tables explain the operation of the circuit diagram.

OR

3 (a) Draw the circuit diagram of basic TTL NAND gate and explain the three parts with the help of functional operation.
(b) Explain the following terms with reference to TTL circuit:
(i) Logic levels. (ii) DC noise margin. (iii) High state fan-out.

UNIT – II

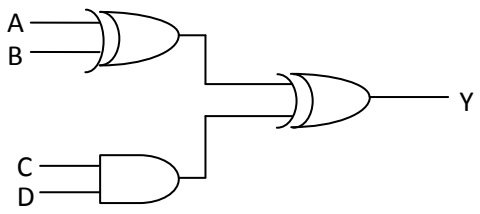
4 (a) Explain about dataflow design elements of VHDL.
(b) Explain the difference in program structure of VHDL and any other procedural language. Give an example.

OR

5 (a) Give the syntax and structure of a package in VHDL.
(b) Write a process based VHDL program for the prime-number detector of 4-bit input and explain the flow using logic circuit.

UNIT – III

6 Obtain logical expression for the logic circuit shown and build the function with 8 to 1 (74x151) multiplexer. Assume BCD are select lines of 74x151.



OR

7 Design a 4x4 combinational multiplier and write the VHDL program in data flow model.

Contd. in page 2

UNIT – IV

8 (a) Draw the logic diagram of IC 74180 parity generator checker and explain its operation with the help of a truth table.

(b) With neat, sketch explain Barrel shifter.

OR

9 (a) Explain how a JK-flip-flop can be constructed using a T-flip-flop.

(b) Give a VHDL code for a 4-bit up counter with enable and clear inputs.

UNIT – V

10 Write short notes on the following:

(a) Two dimensional decoding.

(b) Read / write operation of DRAM.

OR

11 Determine the ROM size needed to realize the logic function performed by 74x153 and 74x139.

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