Code: 13A04303

R13

B.Tech II Year I Semester (R13) Supplementary Examinations November/December 2017

SWITCHING THEORY & LOGIC DESIGN

(Common to ECE & EIE)

Time: 3 hours Max. Marks: 70

PART – A

(Compulsory Question)

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1 Answer the following: (10 X 02 = 20 Marks)

(a) What are the universal gates? Why they are called universal gates?

(b) What do you understand by the term digital systems?

(c) What is the need of K map?

(d) Implement the following function using NANAD gate.

$F = A(B + CD) + (BC)'$

(e) Explain about the combinational circuit with an example.

(f) List out the applications of multiplexer.

(g) Compare shift registers and ripple counters.

(h) What are the advantages of sequential circuits?

(i) What is the basic difference between PLA and PAL.?

(j) What are programmable memories?

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT – I

2 Define prime implicant and essential prime implicants of a Boolean expression. Also, explain about various basic theorems and properties of Boolean algebra.

OR

3 State and prove DeMorgan's law. Also, explain in detail about binary codes and signed binary numbers.

UNIT – II

4 Simplify the following Boolean function using four variable maps

(a) $F(w, \mathrm{x}, \mathrm{y}, \mathrm{z}) = \Sigma(1,4,5,6,12,14,15)$.

(b) $F(A, \mathrm{B}, \mathrm{C}, \mathrm{D}) = \Sigma(0,1,2,4,5,7,11,15)$.

OR

5 Minimize the following function using K-map and also verify through Tabulation method.

$F(A, \mathrm{B}, \mathrm{C}, \mathrm{D}) = \Sigma\mathrm{m}(1,4,5,7,8,9,12,14) + \mathrm{d}(0,3,6,10)$

UNIT – III

6 Define decoder and explain the principle involved in it. Construct 3x8 decoder using logic gates and truth table.

OR

7 Define encoder and explain the principle involved in it and design octal to binary encoder.

UNIT – IV

8 Convert:

(a) JK flip flop to T flip flop.

(b) RS flip flop to D flip flop.

OR

9 Explain in detail about registers and counters with an example.

UNIT – V

10 Illustrate how a PLA can be used for combinational logic design with reference to the functions.

$F1(A, \mathrm{B}, \mathrm{C}) = \Sigma(0, 1, 3, 4)$

$F2(A, \mathrm{B}, \mathrm{C}) = \Sigma(1, 2, 3, 4, 5)$

Realize the same assuming that 3*4*2 is available.

OR

11 What is race condition? How it can be avoided? Also, discuss in detail about error detection and correction.

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